SYNOPSIS OF

DESIGN AND DEVELOPMENT OF ADVANCED NUMERICAL DISTANCE RELAYING TECHNIQUES

A THESIS

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1 Introduction

Protective relays serve as a backbone to the power system. A century old protection technique has recently transformed itself into fourth generation technology, a massive development from i) electromechanical to static, ii) static to digital and from iii) digital to numerical and wide area protection. In 1960 Rockefeller [1] suggested the use of digital computers to protect power system equipments and this opened up a new area in digital protection. This pioneering work attracted many researchers which finally led to the developments in algorithms and filters which are targeted towards digital implementation. In fourth generation technology protective relays, all the logics, techniques and filters are implemented numerically. It also provides scope for development of sophisticated algorithms to assist the distance algorithm for intelligent trip decision. This led to the wide spread use of intelligent electronic device (IED) throughout the power system network, right from generation, transmission and sub-transmission to distribution.

Transmission lines are typically protected by distance protection and it has been serving this task for at-least a century. Numerical distance relay (NDR) protecting transmission lines receives two 3 phase inputs i.e voltage from capacitor voltage transformer (CVT) and current from current transformer (CT). NDR processes these inputs and estimates the apparent impedance. If the estimated impedance is within the set zone of protection, tripping signal is forwarded to the corresponding pole/breaker as set in the protection logics. It may appear to be simple, however it is very difficult to achieve high speed and accurate estimation of apparent impedance of the protected line. This is due to factors like, fault resistance, remote end in-feed, high source to line reach impedance ratio (SIR) and CVT transients which may cause NDR to mal-operate i.e., over-reach or under-reach [2]. This mal-operation may result in system stability issues and damage to equipments which may lead to safety issues.

1.1 Motivation

This research work focuses on developments in numerical distance protection where four different problems i.e., delay in total fault clearing time (TFCT) due to time delay in communication medium or failure of communication medium, relay mal-operation due to CVT transients, estimation of electronic ferro resonance suppression circuit (FSC) resistance and protection of series compensated parallel transmission (SCPTL) lines are discussed.
Distance relay is typically assisted by tele-protection schemes to reduce the TFCT. However, this involves cost due to communication infrastructure. The currently available technique which is still serving the utility is the loss of load protection [3] which is used to accelerate tripping when communication medium is not available or failed. The major limitation is that, it covers all fault types except three-phase fault, as the idea is to detect loss of load current in the healthy phases. This has motivated the need to develop and test accelerated trip logic in real time which can detect balanced faults and can be used along with the existing distance algorithms.

Capacitor voltage transformer is typically used to measure voltages at extra high voltage level because of economic reasons. The fault information delivered by CVT may result relay mal-operation if transients are close to fundamental frequency. Distance relay mal-operation due to potential device transients was first reported in AIEE committee report [4]. Even though transient phenomenon in CVT was existing before, it was not brought to notice due to the slow response time of electromechanical relays. On the other hand, NDR offers half to one full cycle range high speed tripping which emphasized the issue due to CVT transients. This led to the birth of digital CVT models and new techniques/logic to assist the distance algorithm for intelligent trip decision [5, 6, 7, 8]. Most of the techniques proposed were focused to either adaptively reduce zone 1 reach or to provide fixed time delay. Other proposed algorithms are obtained by using simplified CVT model. These factors motivated the research for a cost effective, system independent, simple, and adaptive blocking logic.

Recently, CVT with electronic FSC was proposed [9], where passive FSC was replaced with electronic FSC. The damping resistance value in electronic FSC was estimated by trial and error method. Moreover, the obtained damping resistance values were not validated for ferro-resonance test and transient response test [10] by digital simulation. This motivated the need to estimate damping resistance and test it as per the standard.

In the case of transmission line with series compensation, NDR is prone to mal-operate due to factors like voltage inversion, current inversion and sub-synchronous resonance [11]. Even though memory polarization is currently available to handle inversion issue, sub-synchronous resonance is still a bottle-neck. The existing zone settings for protecting series compensated single line may degrade the NDR performance in the presence of parallel line with series compensation. In order to estimate the zone reach setting, utility has to estimate the steady state and transient errors encountered. This factor motivated to analyze the relay behaviors which
are used to protect SCPTL.

1.2 Objectives of the Work

The main objectives of the research work are:

1. To design assisting logics for numerical distance relay, which can be implemented without any modification in hardware and existing algorithms. The logics are,
   (a) Accelerated trip logic - To accelerate tripping time for balanced faults when communication medium fails or when communication time is high
   (b) Adaptive blocking logic - To prevent mal-operation of distance relay due to CVT transients

   Implementation of above logics along with existing distance relay algorithm in field programmable gate array (FPGA) to test the performance in real time.

2. Estimation of damping resistance for electronic FSC and to test the performance in real time

3. Estimation of steady state error encountered by distance relay for single phase to ground fault (SPGF) in SCPTL.

1.3 Scope of the Work

The scope of the work is limited to the protection of transmission lines by distance relays, which are given as follows

1. The assisting logics i.e., accelerating logic and adaptive blocking logic are individual logic blocks which can be implemented along with existing distance protection without any modification in existing distance algorithm.

2. Testing the performance of estimated damping resistance for ferro-resonance and transient response test are limited to digital simulations. Whereas, the performance of NDR for estimated resistance is tested in real time using FPGA.

3. The other part of the work which analyzes the distance relay steady state error is limited to the protection of SCPTL terminated at same buses at both ends. The analysis is limited to steady state error for SPGF under the assumption that capacitor is not bypassed by air gap or metal oxide varistor, which is the case for low fault current levels.

2 Description of Research Work

The performance of assisting logics and the performance of CVT with electronic FSC has to be tested in real time before field implementation, as direct implementation without testing may
lead to catastrophic equipment damages. This demands for a power system modeling where every individual element in the network is modeled to mimic its behavior depending upon the requirements. In this research work, Alternative Transient Program (ATP) is used to model the entire power system. This includes CVT model [5], CT model [12], arc modeling [13], bus bar model and frequency dependent line modeling [14] for transmission line. In order to test the performance, the protection algorithm in existing IEDs has to be updated, but this cannot be done as details regarding hardware and software are not available and are proprietary. This is overcome by first designing and testing the existing distance algorithm in FPGA.

2.1 Numerical Distance Relay Design

The existing distance relay algorithm along with the most important features are first developed in Xilinx spartan 3A DSP 3SD1800A-FG676. The extracted fault information \( (v_{r,y,b}, i_{r,y,b}) \) is then played to the relay which involves both real and non real time operations as shown in Figure 1. As the aim is to test the performance of assisting logics and electronic FSC in real time, analog signal processing i.e. anti-aliasing filter, sampling and digital signal pre-processing (filtering to remove dc offset) are done using MATLAB. The signals after pre-
processing are then scaled down, converted to signed 16 bit and finally converted to HEX format. The fault information is then stored in FPGA memory and later used for processing by relay. This relay incorporates the most important modules as shown in Table I. The complete design of NDR is done using hardware description language (HDL) Verilog coding and Xilinx ISE-12.1 WebPACK is used to synthesize and implement the design in FPGA.

### Table I  Distance relay modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Discrete Fourier transform</td>
<td>to estimate phasors</td>
</tr>
<tr>
<td>Sequence transformation</td>
<td>to estimate sequence parameters</td>
</tr>
<tr>
<td>Polarizing quantity</td>
<td>to estimate polarizing phasors</td>
</tr>
<tr>
<td>Ground elements</td>
<td>to estimate positive sequence impedance</td>
</tr>
<tr>
<td>Phase elements</td>
<td>to estimate positive sequence impedance</td>
</tr>
<tr>
<td>Security counter</td>
<td>to prevent mal-operation</td>
</tr>
</tbody>
</table>

3  **Accelerated Trip Logic**

This subsection presents the AT logic which is to be included in sending end relay and receiving end relay. Figure 2 shows the logic which will assert the AT signal. This AT signal will be acting as an input to the existing permissive under-reach transfer trip scheme (PUTT) communication scheme as shown in Figure 2. In order to test the performance of AT logic in real

![Fig. 2 Accelerated trip logic along with existing PUTT scheme](image)

- \( R_{Z2}, Y_{Z2}, B_{Z2} \)  Zone 2 ground elements
- \( V_2, I_2 \)  negative sequence phasor
- \( V_0, I_0 \)  zero sequence phasor
- \( Z_{est} \)  estimated positive sequence impedance
- \( RY_{Z2}, YB_{Z2}, BR_{Z2} \)  Zone 2 phase elements
- \( V_{2th}, I_{2th} \)  negative sequence threshold
- \( V_{0th}, I_{0th} \)  zero sequence threshold
- \( Z_{actual} \)  actual positive sequence impedance
time, test system shown in Figure 3 is considered. The extracted fault information for 170km, 180km, 190km and 200km for a particular value of SIR (0.25) and loading condition ($\delta_s = 30$) is played to sending end relay ($R_s$), receiving end relay ($R_r$) and the signals are captured using 4 input channel oscilloscope. Operating time delays with and without AT logic obtained using hardware are shown in Table II (excluding circuit breaker operating time). Since the signal transmission time can be as high as 45ms [15] without including the signal propagation time, communication delay is assumed to be 45ms. It can be observed that there is a considerable reduction in total fault clearing time when AT logic is incorporated along with the existing communication scheme.

<table>
<thead>
<tr>
<th>Fault location (km)</th>
<th>Operating time(ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_r$</td>
</tr>
<tr>
<td>170</td>
<td>19</td>
</tr>
<tr>
<td>180</td>
<td>19</td>
</tr>
<tr>
<td>190</td>
<td>19</td>
</tr>
<tr>
<td>200</td>
<td>19</td>
</tr>
</tbody>
</table>

4 CVT Transient Detection Logic

In order to handle the issue of distance relay mal-operation due to CVT transients, the requirement is to extract the CVT transients i.e., the filter should provide good attenuation at fundamental frequency. Transfer function of the proposed filter in $z$ domain ($z$) for which the required output is CVT transients is shown in equation (1) which is obtained for a sampling rate of 600 Hz.

$$H(z) = 0.5 + 0.5z^{-6}$$

(1)
Magnitude response of this filter shown in Fig. 4 confirms that this filter meets this requirement. It is also necessary that the transient information is available as soon as possible to block the trip signal due to over-reach. The proposed logic which performs this task is shown in Fig. 5 where $R_{Z1}, Y_{Z1}, B_{Z1}$ are ground elements, $RY_{Z1}, YB_{Z1}, BR_{Z1}$ are phase elements and SC is the security counter. In order to perform this task, filter shown in equation (1) is used to extract the unwanted information ($V_{rf}, V_{yf}, V_{bf}$) from the voltage samples ($V_r(t), V_y(t), V_b(t)$) which are obtained after prepossessing using anti-aliasing filter. The extracted information is compared with both lower ($V_{lth}$) and upper ($V_{uth}$) bounds, since the output of PF ($V_{rf}, V_{yf}, V_{bf}$) will be almost zero during normal operating condition or when CVT transients dies out completely. The performance of the proposed logic is tested for different fault types and loading conditions for remote end faults. In addition to this, the real time performance of the proposed logic for close-in faults is also tested.
5 Estimation of resistance for CVT with Electronic FSC

The transient response of instrument transformers affects the performance of high speed relays, particularly speed and over-reach in case of distance protection. Transient response of CVT depends on the type of FSC, provided in CVT secondary to damp the ferro resonant oscillations as shown in Fig. 6. Fig. 7 shows the model of electronic FSC used in Fig. 6. In order to estimate this resistance ($R$), transfer function of the CVT shown in Figure 6 is obtained [5], but without simplification as in [5]. The transfer function of CVT model is shown in equation (2).

\[
G(s) = \frac{N_3s^3 + N_2s^2}{D_5s^5 + D_4s^4 + D_3s^3 + D_2s^2 + D_1s + D_0}
\]  

where $N_3, N_2, D_5, D_4, D_3, D_2, D_1$ are the coefficients expressed by CVT parameters. The requirement is to have low time constant, so that the protective relays are exposed to the actual desired information immediately after fault inception. This is achieved by estimating damping resistance ($R_{est}$) which will give low time constant by using equation (3).

\[
TC_{min} = \min \left( \max \left( T_{1R}, T_{2R}, T_{3R}, T_{4R}, T_{5R} \right) \right)_{R=1,2,...,10000}
\]  

Fig. 6 Detailed model of CVT

\[C_1, C_2\text{ stack capacitance} \quad RC, L_C\text{ tuning resistance and inductance} \]

\[SW_1, SW_2\text{ switches} \quad RB\text{ relay burden} \]

\[R_{T1}, L_{T1}, C_T, R_{TC}, L_{TC}, R_{T2}, L_{T2}\text{ parameters of intermediate transformer} \]
where \( T_{1R}, T_{2R}, T_{3R}, T_{4R}, T_{5R} \) are the time constants of the transfer function \( G(s) \) for a particular value of damping resistance \( R \). Figure 8 is obtained from equation (3), where maximum time constant of the transfer function is obtained for each value of resistance. The CVT with estimated resistance for electronic FSC is tested for ferro-resonance and transient response test [10] and the results are found within the limits. The performance of CVT is also tested in real time. In addition to this, the performance of CVT with estimated resistance is also compared with existing techniques for different source to line reach impedance ratio, fault types and loading conditions.

6 Protection of Series Compensated Transmission Lines

Distance relay zone reach setting demands the knowledge of transient and steady state error to ensure secure operation. The knowledge of this steady state error is important, as this gives initial information regarding reach setting for ground and phase elements, above which the transient errors are considered to decide the final reach setting in distance relay. From utility perspective, it helps protection engineers to analyze the steady state relay behavior by providing the basic sequence impedance information, which is estimated for a particular tower configuration. In order to analyze the steady state error and behavior of distance relays A, B, C in the presence of series capacitor, test system shown in Fig. 9 is considered. Expressions to estimate impedance for both with and without zero sequence mutual compensation are derived considering different factors i.e., fault resistance, remote end in-feed, capacitor located at one
Fig. 9  Conventional distance relay protecting SCPTL

G Generator
$Z_M, Z_S$ Source impedance
CB Circuit breaker
$m$ Fault location in pu
$F_1$ Single phase to ground fault (SPGF)
$I_S$ In-feed from receiving end for SPGF
$I_M$ In-feed from sending end for SPGF
$V_R$ Voltage phasor estimated by relay

$\delta_S$ Loading angle sending end
$Z_L$ Line impedance
$\delta_R$ Loading angle receiving end
$C$ Capacitor
$I_R$ Current phasor estimated by relay

end and for capacitor located at both ends. In order to assist the analytical expressions, the actual relay behavior for two different tower configurations for each of the above mentioned cases are discussed. The capacitors are assumed to be located at the end of the line, which is mostly the case in real world scenario. This is due to the fact, that mid-point capacitors will incur additional installation cost (if substation does not exist) when compared to capacitors located at the end of the line. Out of the ten different fault types (3 SPGF, 3 phase to phase fault, 3 phase to phase and ground fault and 3 phase fault), fault involving ground is chosen, as the impact of coupling on distance relay is significant in zero sequence. SPGF is considered, because probability of its occurrence is more when compared to phase to phase and ground fault.

7 Summary and Conclusions

The work can be summarized as follows:

1. Distance relay assisting logics
(a) Accelerated trip logic reduces the TFCT for balanced faults. This will not affect the performance of existing schemes as there is no information exchange between AT logic and the present schemes. This logic is simple and is practically feasible for implementation without any hardware modification. Real time testing is carried out for different fault locations to monitor its performance.

(b) Adaptive blocking logic blocks the distance relay mal-operation when transients is detected and unblock the distance relay mal-operation when transients decay. Testing is carried out at high SIR for different fault types, loading condition. In addition to this real time performance of the logic is also verified for close-in faults.

2. Estimation of resistance for CVT with electronic FSC is done using transfer function of detailed CVT model. Real time testing is carried out to verify the performance of CVT with existing method. In addition to this the performance of CVT with electronic FSC is analyzed for different fault types, loading condition and SIR with existing FSC.

3. Analytical expressions are derived to estimate steady state error for different conditions for the protection of SCPTL.

The important conclusions of the work are:

1. Distance relay assisting logics
   (a) The advantage of the AT logic is suitable for system, where communication medium is other than the fiber optic cable or if the medium fails. If stability is the major concern for the utility to switch to costly communication medium, then AT logic will be a cost effective solution

   (b) The adaptive blocking logic monitors the CVT transients directly in time domain unlike any other approach where the transients are indirectly monitored in frequency domain. This saves time to detect transients as transforming information from time domain to frequency domain involves delay. Moreover, since the transients are directly monitored, it does not need any SIR threshold which are automatically derived in background using relay settings

2. CVT with electronic FSC
   The CVT with estimated resistance is tested for transient response test and ferro resonance test as per the standard and the errors are found within the limits. CVT with electronic FSC shows better transient response when compared with existing techniques. This results in distance relay exposed to actual primary fault information relatively fast and with less error. Analysis shows that the performance of CVT with electronic FSC is better for high SIR, however the improvement is minimal

3. Steady state error in SCPTL protection
   The prior availability of sequence impedance information for relay setting helps the utility to estimate steady state error and study the relay behavior by direct substitution. These expressions helps to provide primary information to the utility in deciding zone 1 reach setting, before considering safety factor for zone reach setting to accommodate transient errors.
References


8 Proposed Contents of the Thesis

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9 Publications

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Accepted


**Under 2nd Revision**


**Communicated**


**9.2 Conference**

**International**


**National**